IN THE CLAIMS

Please amend the claims as follows:

Claim 1 (Currently Amended): A semiconductor device comprising:

an active area of a MOSFET separated by an element isolation area on a semiconductor substrate;

at least one gate electrode provided to pass over the active area; and

at least one source/drain contact formed on a surface of the active area at one side of the gate electrode,

wherein the gate electrode has a shape to vary so that a gate length decreases with increasing a distance from a position of the source/drain contact along the gate electrode, and one gate electrode is provided in the active area, and source/drain contacts are arranged at respective sides of the gate electrode at diagonal positions in the active area.

Claim 2 (Canceled).

Claim 3 (Currently Amended): The semiconductor device according to claim [[2]] 1, wherein the MOSFET is one of a PMOSFET and an NMOSFET of a CMOS inverter.

Claim 4 (Original): The semiconductor device according to claim 1, wherein one gate electrode is provided in the active area, and source/drain contacts are arranged at one end of the gate electrode in a channel width direction.

Claim 5 (Original): The semiconductor device according to claim 1, wherein the gate electrode has a planar pattern such that the gate length varies in a laterally symmetrical form.

Claim 6 (Original): The semiconductor device according to claim 1, wherein the gate electrode has a planar pattern such that the gate length varies in a laterally asymmetrical form.

Claim 7 (Original): The semiconductor device according to claim 1, wherein a silicide layer is formed on the surface of the active area at the opposite sides of the gate electrode, and the source/drain contact is in contact with the silicide layer.

Claim 8 (Original): A semiconductor device comprising:

an active area separated by an isolation area on a semiconductor substrate and in which a plurality of MOSFETS are arranged so as to be connected in series in the active area;

a plurality of gate electrodes juxtaposed with each other so as to pass over the active area;

a first source/drain contact formed at a side of the juxtaposed gate electrodes and in contact with a surface of the active area, and

a second source/drain contact formed at another side of the juxtaposed gate electrodes and in contact with a surface of the active area,

wherein the shape of the gate electrode located closest to one of the first and second source/drain contacts is formed to vary step by step or continuously so that a gate length decreases with increasing a distance from a position of one of the first and second source/drain contacts along the gate electrode.

Claim 9 (Original): A semiconductor device according to claim 8, further comprising at least one intermediate source/drain contact formed in contact with a source/drain area of an

intermediate MOSFET corresponding to an intermediate one of the plurality of gate electrodes, and

wherein the gate electrode located closest to the intermediate source/drain contact has a shape formed to vary step by step or continuously so that the gate length decreases with increasing distance from the position of the intermediate source/drain contact along the gate electrode.

Claim 10 (Original): The semiconductor device according to claim 8, wherein the plurality of MOSFETS form a NAND type memory unit in a NAND type flash memory.

Claim 11 (Original): The semiconductor device according to claim 8, wherein the first and second source/drain contacts arranged at the respective sides of the gate electrode are arranged at diagonal positions in the active area.

Claim 12 (Original): The semiconductor device according to claim 8, wherein the first and second source/drain contacts arranged at the respective sides of the gate electrode are arranged at the same end of the gate electrode in a channel width direction.

Claim 13 (Original): The semiconductor device according to claim 8, wherein the gate electrode has a planar pattern such that the gate length varies in a laterally symmetrical form.

Claim 14 (Original): The semiconductor device according to claim 8, wherein the gate electrode has a planar pattern such that the gate length varies in a laterally asymmetrical form.